REMARKS/ARGUMENTS

In the Office Action mailed February 25, 2010, claims 1-23 were rejected. In response, Applicants hereby request reconsideration of the application in view of the amendments and the below-provided remarks. No claims are amended, added, or canceled.

For reference, claims 1, 7-12, and 18-22 are amended. In particular, claim 1 is amended to clarify the locations of certain structural limitations relative to the coprocessor. In particular, the first counter, second counter, control means, and output means are implemented within the coprocessor, while the FIFO memory and the controller are located remotely from the coprocessor. Similar amendments are presented for claims 7, 12, and 18 (although claims 7 and 18 refer to the third counter, fourth counter, and input means, rather than the first counter, second counter, and output means). These amendments are supported by the subject matter illustrated in Figs. 1-3, along with the accompanying subject matter described in the specification. In particular, Fig. 1 shows an implementation of a multiprocessing computer system in which the controller 4 and the FIFO memory (memory banks 1) are located remotely from the coprocessors 2. Fig. 2 shows an implementation of a writing device which includes a first counter, second counter, control means, and output means for implementation within a coprocessor 2. Fig. 3 shows an implementation of a writing device which includes a third counter, fourth counter, control means, and input means for implementation within a coprocessor 2. Claims 1, 7, 12, and 18 are also amended to clarify that the data elements are at least part of a communication between the coprocessor and the controller in the multiprocessing environment. These amendments are supported, for example, by the subject matter described at page 2, lines 23-24, of specification of the present application. Claims 7-11 and 18-22 are also amended to clarify the language of the claim by deleting step language.

Claim Rejections under 35 U.S.C. 103

Claims 1-23 were rejected based on one or more cited references. The cited reference(s) relied on in these rejections include:

Robertson (U.S. Pat. No. 6,892,253, hereinafter Robertson)

Myers (U.S. Pat. Pub. No. 2002/0146023, hereinafter Myers)

Bender et al. (U.S. Pat. No. 5,664,223, hereinafter Bender)

In particular, claims 1-23 were rejected under 35 U.S.C. 103(a) as being unpatentable over Robertson in view of Myers further in view of Bender. However, Applicants respectfully submit that these claims are patentable over Robertson, Myers, and Bender for the reasons provided below.

Independent Claim 1

Claim 1 is patentable over the combination of Robertson, Myers, and Bender because the combination of cited references does not teach all of the limitations of the claim. Claim 1 recites:

> Device for writing data elements from a coprocessor into a FIFO memory, in a multiprocessing environment comprising at least one coprocessor, a FIFO memory and a controller, said device comprising:
>
> a first counter implemented within the coprocessor, the first counter for counting the available room in said FIFO memory, wherein the FIFO memory is located remotely from the coprocessor;
>
> a second counter implemented within the coprocessor, the second counter for counting the number of data elements written into said FIFO memory, wherein the data elements are at least part of a communication between the coprocessor and the controller in the multiprocessing environment;
>
> control means implemented within the coprocessor and coupled to the first and second counters, wherein the control means is configured for checking said first counter for available room in said FIFO memory, for checking said second counter whether a predetermined number N of data elements have been written into said FIFO memory, for decrementing the count of said first counter and for incrementing the count of said second counter after a data element has been written into said FIFO memory; and
>
> output means implemented within the coprocessor, the output means for outputting data elements to said FIFO memory, wherein the

output means comprises a first connection to the control means, a second connection to the FIFO memory, and a third connection to the controller, wherein the control means connects between the counters and the output means, and the output means connects between the control means and the controller;

wherein said control means is adapted to issue a first message when the count of said second counter has reached said predetermined number N by incrementing of the count of said second counter after a data element has been written into said FIFO memory;

wherein said control means is adapted to issue a first call for available room in said FIFO memory to said controller; and

wherein said output means is adapted to forward said first message and said first call to said controller, wherein the controller is located remotely from the coprocessor.

(Emphasis added.)

In contrast to the language of the claim, the combination of cited references does not teach the overall arrangement recited in the claims. The failure of the combination of cited references to teach the overall arrangement recited in the claims is understandable because the systems described in the cited references are directed to different uses and operation compared with the embodiments recited and described in the present application.

The teachings of Robertson illustrate this general difference between the overall arrangements of the cited references and the present application. The present application is directed to communications within a multiprocessing environment. In contrast, Robertson does not teach any type of communications within a multiprocessing environment. Rather, Robertson is merely directed to a data transfer controller which maintains a status of a first-in-first-out (FIFO) buffer 410. Robertson, abstract. The transfer controller connects various memory port nodes for transferring data. Robertson, col. 2, lines 28-30. However, Robertson does not teach using the transfer controller in a multiprocessing environment.

In addition to the general differences between the overall environment of the present application and Robertson, the specific teachings of Robertson also fail to address all of the limitations of the claim. In particular, although Robertson describes several operations for data transfer, the described functionality and corresponding structural elements which facilitate the data transfer are specifically implemented within the

transfer controller of Robertson. The indicated functionality and corresponding structural elements are not implemented by a coprocessor within a multiprocessing environment. Therefore, since the counters and other elements of Robertson are specifically implemented within the transfer controller, Robertson fails to teach implementing the described counters and other elements within a coprocessor of a multiprocessing environment.

For the reasons presented above, the combination of Robertson, Myers, and Bender does not teach all of the limitations of the claim at least because the cited references (namely Robertson) do not teach the overall arrangement recited in the claims and, more specifically, do not teach implementing the indicated functionality and corresponding structural elements within a coprocessor within a multiprocessing environment, as recited in the claim. Accordingly, Applicants respectfully assert claim 1 is patentable over the combination of Robertson, Myers, and Bender because the combination of cited references does not teach all of the limitations of the claim.

Independent Claims 7, 12, and 18

Applicants respectfully assert independent claims 7, 12, and 18 are patentable over the cited references at least for similar reasons to those stated above in regard to the rejection of independent claim 1. Each of these claims recites subject matter which is similar to the subject matter of claim 1 discussed above. Although the language of these claims differs from the language of claim 1, and the scope of each claim should be interpreted independently of other claims, Applicants respectfully assert that the remarks provided above in regard to the rejection of claim 1 also apply to the rejections of these claims.

Dependent Claims

Claims 2-6, 8-11, 13-17, and 19-23 depend from and incorporate all of the limitations of the corresponding independent claims 1, 7, 12, and 18. Applicants respectfully assert these dependent claims are allowable based on allowable base claims. Additionally, each of these dependent claims may be allowable for further reasons.

CONCLUSION

Applicants respectfully request reconsideration of the claims in view of the amendments and the remarks made herein. A notice of allowance is earnestly solicited.

This response is accompanied by the appropriate fee to obtain a 3-month extension of the period for responding to the Office Action, thereby moving the deadline for response from May 25, 2010, to August 25, 2010.

At any time during the pendency of this application, please charge any fees required or credit any over payment to Deposit Account **50-4019** pursuant to 37 C.F.R. 1.25. Additionally, please charge any fees to Deposit Account **50-4019** under 37 C.F.R. 1.16, 1.17, 1.19, 1.20 and 1.21.

Respectfully submitted,

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Date: August 25, 2010

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